REMARKS

Claims 1, 14 and 27 are amended. Claims 2, 15, and 28 are cancelled. Claims 1, 3-14, 16-27 and 29-39 are pending in the present application.

Claims 1, 14 and 27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,776,645 ("Barr"). Applicants respectfully traverse this rejection.

Claim 1, as amended, recites a method for measuring the registration between at least two integrated circuit layers comprising, *inter alia*, "determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location, wherein at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers." Barr does not disclose all of these limitations.

Barr discloses a method for measuring overlay between two lithographic patterns that use a pre-defined "print bias target pattern." The "print bias target is made up of a pair of concentric geometric shapes in which a plurality of target regions forms a plurality of isolated edges." Abstract; Col. 14, lines 5-28. Therefore, the print bias target of Barr is a target pattern having no function on the integrated circuit layer, added only for overlay measurements and not "a non-metrological structure on said one of said integrated circuit layers," as recited in amended claim 1.

The present invention offers many benefits over the Barr method. One such benefit is increased miniaturization of the integrated circuit chip by eliminating special "target patterns." Another benefit is that since the present invention uses the actual circuit patterns to measure overlay, alignment errors between the "target patterns" in

the scribe lane with respect to the actual circuit pattern (which are generally written separately from the scribe lane) may be eliminated.

Likewise, claim 14, as amended, recites that "at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers." Claim 27, as amended, recites the same limitation. Bar does not disclose this limitation of claims 14 and 27.

Since Barr does not disclose all the limitations of claims 1, 14 and 27, Barr does not anticipate these claims. Accordingly, Applicants respectfully request that the 35 U.S.C. § 102(b) rejection of claims 1, 14, and 27 be withdrawn.

Claims 1, 3-9, 11-14, 16-22, 24-27, 29-35 and 37-39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over "the combination of Into (US 4,938,600A) and Barr et al. (US 5,776,645A)." Applicants respectfully traverse this rejection.

Into and Barr, whether considered alone or in combination, do not teach or suggest all the limitations of claim 1. In particular, Into and Barr, even when considered together, fail to teach or suggest "determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location, wherein *at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers,*" as recited in claim 1. Emphasis added.

As discussed above, Barr prints a special print bias target for overlay measurement and does not use "a non-metrological structure on said one of said integrated circuit layers" as a reference point.

Likewise, Into discloses using a "box-in-box registration pattern set," rather than a functional feature of the integrated circuit layer. Col. 4, line 31; Col. 6, lines 19-22; Figs. 3A-4B. Moreover, Into's method merely eliminates systematic errors in overlay measurements that are caused by how the measurement tool interprets the target overlay patterns, but does not address overlay errors caused by using special target patterns.

Claims 14 and 27 recite similar limitations as claim 1. Specifically, claims 14 and 27 recite that "at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers."

Since Into and Barr do not teach or suggest all the limitations of claims 1, 14 and 27, these claims and claims 3-9, 11-13, 16-22, 24-26, 29-35 and 37-39 depending therefrom are patentable over the references. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 1, 3-9, 11-14, 16-22, 24-27, 29-35 and 37-39 be withdrawn.

Claims 10, 23, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Into and Barr, and further in combination with U.S. Patent No. 4,766,311 ("Seiler"). Applicants respectfully traverse this rejection.

Claim 10 depends from claim 1. Claim 23 depends from claim 14. Claim 36 depends from claim 27. As discussed above, Into and Barr do not teach or suggest all the limitations of claims 1, 14 and 27. Seiler does not supplement the deficiencies of Into and Barr in this respect. Seiler discloses a method and apparatus for "making precise measurements as small as in submicron distances of an object." (Abstract).

Like Into and Barr, Seiler does not teach or suggest all limitations of any of claim s 1, 14, and 27. Specifically, Seiler fails to teach or suggest "determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location, wherein at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers," as recited in claim 1. Seiler also fails to teach or suggest a "means for digitizing said image and processing said digitized image to determine a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers, wherein at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers," as recited in claim 14. Seiler further fails to teach or suggest "digitizing said top-down image to provide a digitized image, and processing said digitized image to determine a relative location of said first visible feature of said first integrated circuit layer, relative to said second visible feature of said second integrated circuit layer by determining a location of a first feature reference point in said first visible feature of said first integrated circuit layer, and a location of a second feature reference point in said second visible feature of said second integrated circuit layer to indicate said relative location, wherein at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers," as recited in claim 27.

Since Into, Barr and Seiler do not teach or suggest all the limitations of claims 1, 14 and 27, these claims and claims 10, 23 and 36 depending therefrom are patentable over the references. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 10, 23 and 36 be withdrawn.

In view of the above amendment, applicants believe the pending application is in condition for allowance.

Dated: December 15, 2005

Respectfully submitted,

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